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NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Technical Memorandum 33-772

***RAPID—A Random Access Picture Digitizer,
Display, and Memory System***

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PICTURE DIGITIZER, DISPLAY, AND MEMORY
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Technical Memorandum 33-772

***RAPID—A Random Access Picture Digitizer,
Display, and Memory System***

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CALIFORNIA INSTITUTE OF TECHNOLOGY
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May 15, 1976

PREFACE

The work described in this report was performed by the Space Sciences Division of the Jet Propulsion Laboratory.

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ABSTRACT

RAPID is a system capable of providing convenient digital analysis of video data in real-time. RAPID has two modes of operation. The first allows for continuous digitization of an EIA RS-170 video signal. Each frame in the video signal is digitized and written in 1/30 of a second into RAPID's internal memory. This memory is organized as a two-dimensional 256 x 256 array of 8-bit bytes. The second mode leaves the content of the internal memory independent of the current input video. In either mode, a digital processor (computer) can randomly access (read or write) any byte (or word) in RAPID's memory specified by a 16 (15) bit address. The cycle time of that access is about 5 μ s (5 to 7 CPU cycles). In both modes of operation the image contained in the memory is used to generate an EIA RS-170 composite video output signal representing the digitized image in the memory so that it can be displayed on a monitor.

I. INTRODUCTION

The need for a device to provide digital high-speed random access to elements of TV images is well established in the pattern recognition, artificial intelligence and remote sensing research communities. The existing commercial units provide either slow random access of about 1/30 second or require use of constrained and noncommercial camera equipment. Faced with the requirement of real-time analysis of images in the robotics project at JPL, we designed and built RAPID, which is a prototype of the kind of device which is essential to digital real-time analysis of standard video data. The design effort started in May 1975, and was completed in March 1976. We expect to have a working system in June 1976. RAPID will replace the existing video digitizing equipment (also an in-house product) and will substantially replace the RAMTEK RX-100A graphics, gray level and color display system currently used in the robotics project.

The sensors used in the current system are two GE TN-2000 cameras (charge injection solid-state TV cameras). Both cameras are equipped with 50 mm automatic iris lenses. We expect to add another camera equipped with a 12.5-mm lens. The two 50-mm cameras will be used for stereo triangulation and relatively high-resolution analysis; the 12.5-mm-lens camera will be used for wide-area crude observations. No color information is available in the present system.

To allow for the multiplicity of sensors, RAPID is provided with a video selector which can select one of seven video channels for digitization; RAPID locks on an external EIA RS-170 sync signal. Figure 1 gives a broad overview of the visual sensor and RAPID systems.

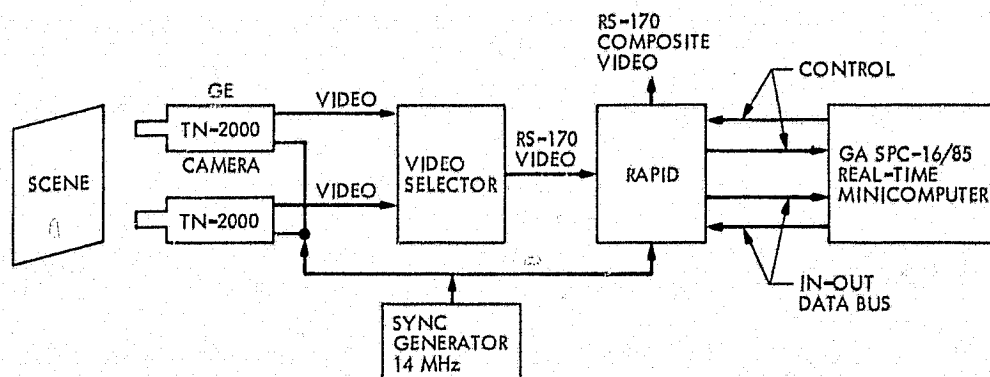


Fig. 1. System overview

II. SENSORS

The TN-2000 has a sensor array of 188×244 photosensitive elements. These elements are scanned by the camera system to generate RS-170 composite video. The video digitization in RAPID is performed in such a way that there are 192×240 digitizations for a full TV scan. RAPID's memory is organized as a 256×256 byte array. Hence, 64 bytes on the right-hand side of each row and the bottom 16 rows are not modified by video data and can be used by the computer and software as an auxiliary memory.

III. RAPID'S MEMORY ADDRESSING SCHEME

RAPID's memory is composed of 128 Mostek MK-4069P-7 chips. These are random access dynamic chips, each containing 4096 bits addressed by a 12-bit address word. The 12-bit address is transmitted in two steps as 6-bit column address and 6-bit row address. The 128 chips are implemented on four identical cards, each containing two blocks, A and B, and each block has two parts, L and R. Each part is composed of 8 chips. A byte is stored on 8 chips of a part with the same 12-bit address. The 8 chips of a part are always accessed in parallel.

The computer addresses a byte by a 16-bit address word which selects the card, block, part, and the address of the chips. The addressing scheme is described in Fig. 2.

The 12-bit address of the bit on the chips corresponds to 6 bit CAD (column address) and 6 bit RAD (row address). The matching is not done

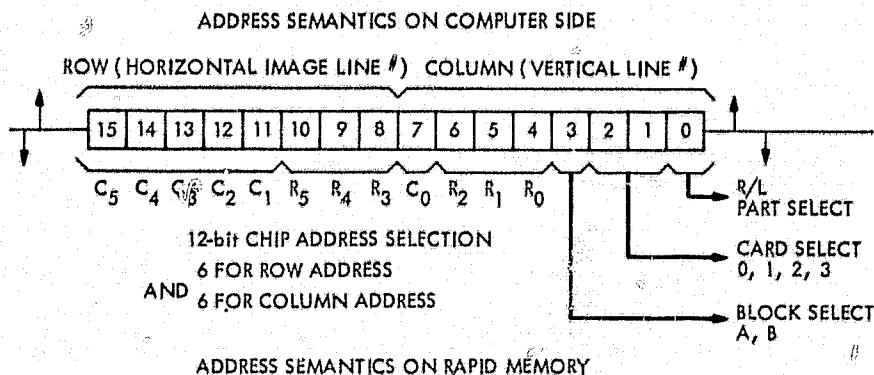


Fig. 2. Addressing scheme

in a straightforward manner because of memory-refreshing constraints (to be discussed later). RAPID's memory can be accessed by the computer also as a 16-bit-word memory device, in which case only a 15-bit address is specified. That is, both R and L bytes are accessed simultaneously.

IV. DIGITIZED VIDEO BUFFERS

The A/D converter of the input video signal operates in the frequency of 3.6 MHz as determined by four 14.318-MHz clock pulses. That is, it sends one (8-bit) byte every 280 ns as dictated by the video scan rate. This rate is faster than the memory cycle (which is at least a minimum of 425 ns); hence the digitized video must be buffered before being stored into RAPID's memory. Two 16-byte buffers were built, one for reading digitized video in, and the other for generating video output. Each of these buffers operates in double buffering mode and allows wide parallel access to RAPID's memory for video I/O (8 bytes in parallel), which releases sufficient time for computer access.

V. DIGITIZED VIDEO INPUT BUFFER ORGANIZATION

The 16-byte input buffer has two identical parts, A and B, used for double buffering. When one part is used for video input, the other part is stored 8 bytes (64 bits) in parallel in one memory cycle on RAPID's memory within 700 ns, as shown in Fig. 3.

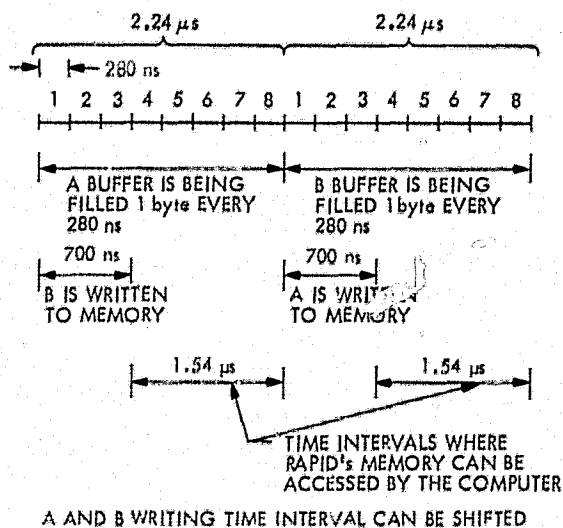


Fig. 3. Input buffer time cycle (when no computer access cycle is in progress on buffer cycle request)

VI. DIGITIZED VIDEO OUTPUT BUFFER ORGANIZATION

The output buffer is organized into two parts, A and B, as is the case with the input buffer. While one part of the buffer is filled with 8 bytes in parallel from memory in 700 ns, the other part (8 bytes) is converted by the D/A converter into video signal at a rate of one byte every 280 ns, as shown in Fig. 4.

In both cases, RAPID's memory is free for 1.54 μ s every 2.24 μ s. During this time, the computer can access the memory. The computer/video memory access scheduling is shown in Fig. 5. If there is a computer access cycle to RAPID's memory in progress when the buffer cycle is requested, the buffer cycle is postponed until the current computer memory cycle is completed (in less than 1 μ s).

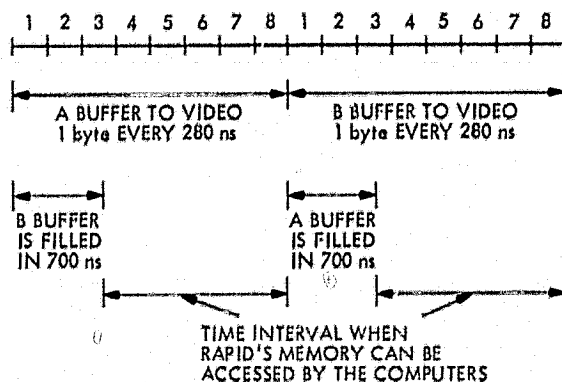


Fig. 4. Video output buffer memory cycle (when RAPID's memory is free on buffer request)

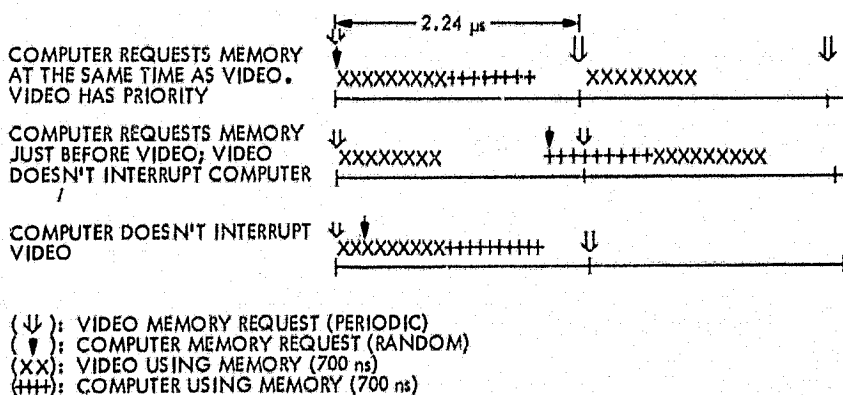


Fig. 5. Memory access conflicts solution

VII. MEMORY REFRESHING

Because the 4096P-7 is a dynamic memory, it has to be refreshed (e. g., each row in the chip must be accessed) every 2 ms. The GE TN-2000 cameras repeat every line twice, hence we are interested in every other line of the odd field or the even field. Only 240 lines and 192 pixels of every line are to be stored in every picture.

When the video input contains a repeated line, this line is not digitized and the memory is refreshed by displaying the proper line that is already in the memory (i. e., digitized video output). In order to refresh every row of the memory, chips row and column addressing is done as shown in Fig. 6. This mapping refreshes every memory row even though the digitized video column number goes up to only 192. The mapping causes the following memory allocation (Fig. 7):

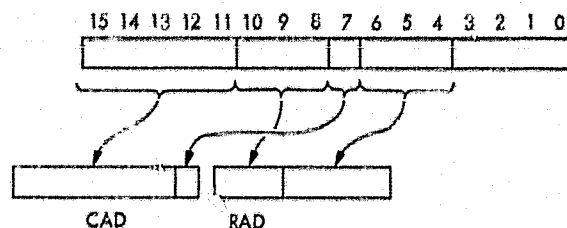


Fig. 6. Chip addressing scheme

| ONE CHIP OF BLOCK A | | | | | | | | | ONE CHIP OF BLOCK B | | | | | | | | |
|---------------------|-------------|----|-----|---|---|---|---|---|---------------------|-------------|----|-----|---|---|---|---|---|
| CHIP ROW | CHIP COLUMN | | | | | | | | CHIP ROW | CHIP COLUMN | | | | | | | |
| | 0 | 1 | 2 | 3 | 4 | - | - | - | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0 | 1 | 17 | 193 | • | • | • | • | • | 0 | 2 | 18 | 194 | • | • | • | • | • |
| 1 | 3 | 19 | • | • | • | • | • | • | 1 | 4 | 20 | • | • | • | • | • | • |
| 2 | 5 | 21 | • | • | • | • | • | • | 2 | 6 | 22 | • | • | • | • | • | • |
| 3 | 7 | 23 | • | • | • | • | • | • | 3 | 8 | 24 | • | • | • | • | • | • |
| 4 | 9 | X | • | X | • | X | • | X | 4 | 10 | X | • | X | • | X | • | X |
| 5 | 11 | X | • | X | • | X | • | X | 5 | 12 | X | • | X | • | X | • | X |
| 6 | 13 | X | • | X | • | X | • | X | 6 | 14 | X | • | X | • | X | • | X |
| 7 | 15 | X | • | X | • | X | • | X | 7 | 16 | X | • | X | • | X | • | X |
| 8 | 25 | 41 | • | • | • | • | • | • | 8 | 26 | 42 | • | • | • | • | • | • |

BEGINNING OF THE 2nd VIDEO LINE
 BEGINNING OF THE 9th VIDEO LINE
 24 BUFFERS = 192 pixels = 1 LINE

NUMBERS INSIDE SQUARES STAND FOR SEQUENTIAL BUFFER NUMBERS WRITTEN ON THAT ELEMENT
 X = CHIP BITS NOT MODIFIED BY VIDEO (RIGHT-HAND SIDE OF VIDEO LINE ELEMENTS 192 THROUGH 236)
 FULL REFRESH WILL OCCUR EVERY 9th LINE

Fig. 7. Memory refreshing for horizontal lines 1 - 240

Figure 7 shows a sample chip of memory part A and a sample chip of memory part B. All chips in the same memory block are addressed similarly. There are 64 chips for each memory block, corresponding to the 64 bits of the corresponding buffer part. The diagram shows the correspondence of the buffer bits onto the memory chips (for writing or reading). The longest time that passes between two refreshings occurs between line number 240 and line 8 (of the next field). The chip portion corresponding to lines 240 through 256 is shown in Fig. 8, which includes the worst case of no refresh period.

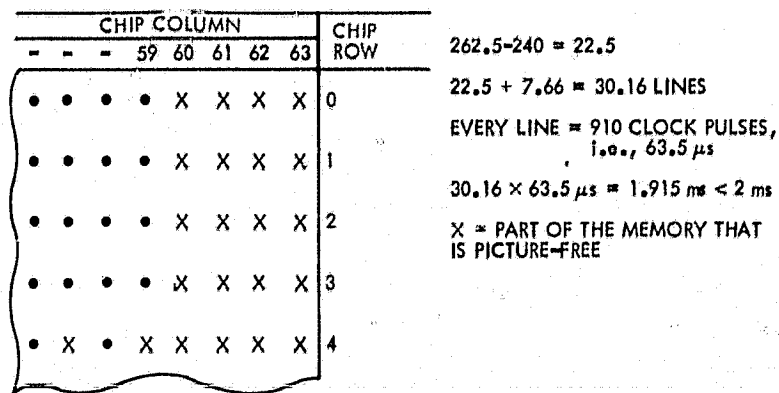


Fig. 8. Addressing for lines 240-256 and worst case no refresh time

VIII. MEMORY CYCLE

As can be seen from the circuit, whenever there is a video-memory request or a computer-memory request, the memory cycle begins unless there is an incompleted cycle in progress. The wave shapes that the memory cycle generates are shown in Fig. 9.

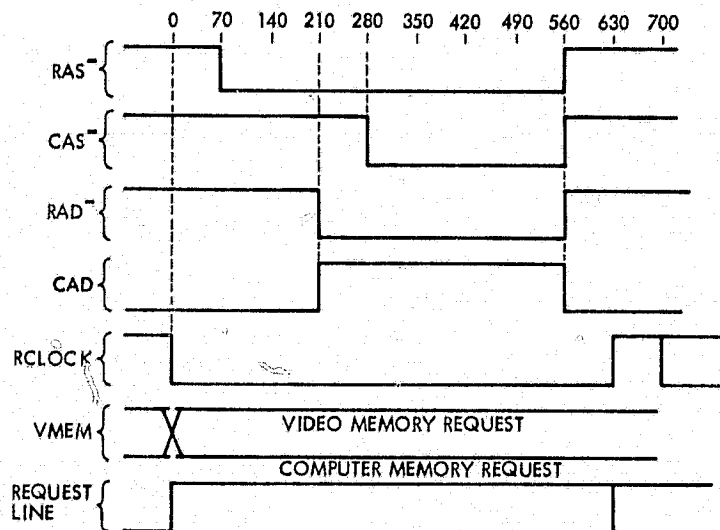


Fig. 9. Wave shapes generated by memory cycle

If the request line remains high even after the cycle is over (which means another request was waiting), it takes 70 ns to reset the RELOCK flipflop, which assures at least 210 ns (125 ns is the minimum lapse of time between two cycles) between two consecutive RAS. Therefore, the memory cycle is 700 ns.

IX. SPC-16 I/O SOFTWARE TO RAPID

CPU-RAPID communication is done by programmed I/O operations with interrupts. In order to access 64-byte memory, we need 16 bits of byte address or 15 bits of word address and 16 (8) lines for word (byte) content. It takes 2 I/O instructions for the SPC-16 CPU, which has a 16-bit I/O bus to "READ" or "WRITE" to the digitizer.

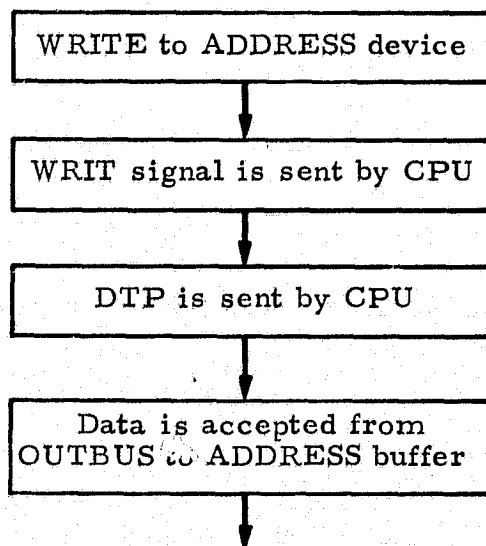
The digitizer represents two different devices for the CPU:

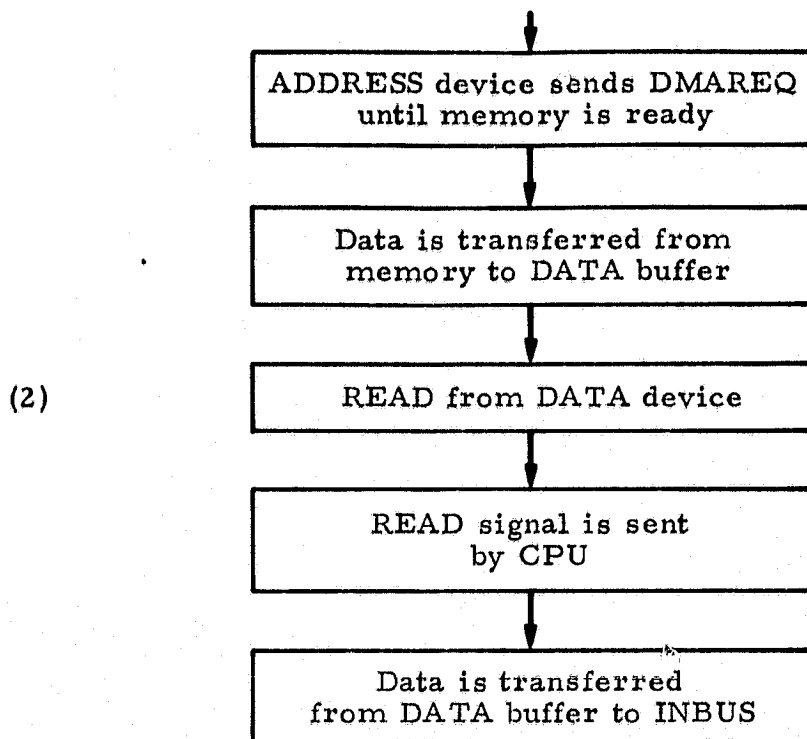
(1) ADDRESS device, and (2) DATA device. RAPID sends a DMA request to CPU to avoid conflicts with other I/O instructions to RAPID. Otherwise a conflicting instruction could change the DATA buffer content.

Both "WRITE" and "READ" to/from the digitizer are executed in two SPC-16 instructions.

"READ" from digitizer

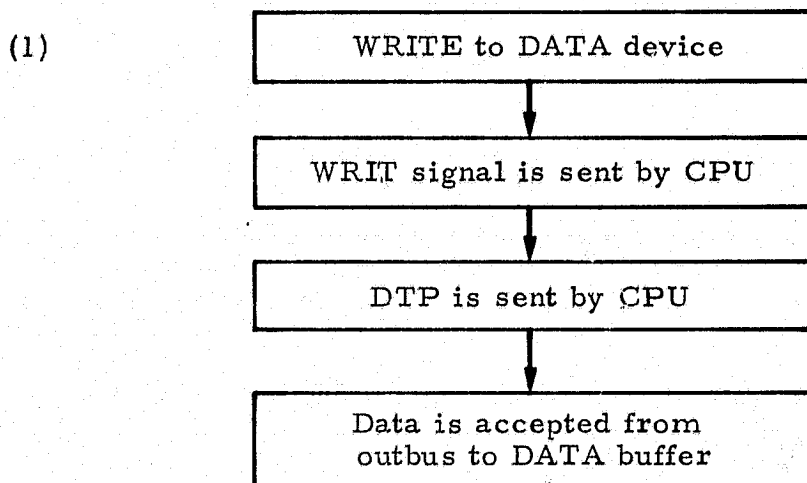
(1)



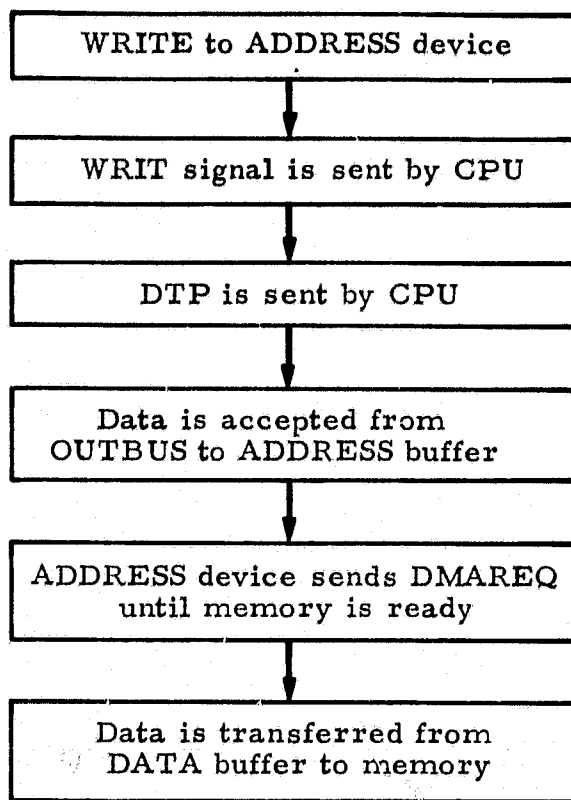


- (1) Write instruction to ADDRESS device with the address of the memory we want to read
- (2) Read instruction to DATA device.

"WRITE" to digitizer



(2)



- (1) Write instruction to data device with content we want to write.
- (2) Write instruction to address device with the address of memory where we want to write

Timing for output to the DATA device is shown in Fig. 10.

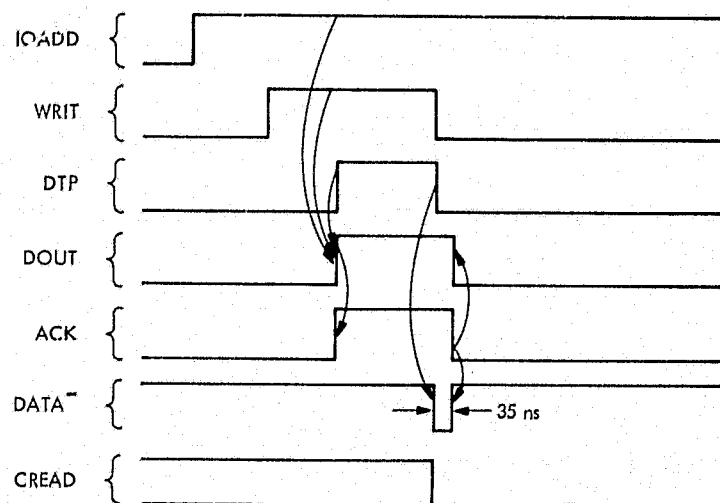


Fig. 10. DATA device output timing

Timing for output to the ADDRESS device is shown in Fig. 11

Output to the DATA device resets the CREAD mode; on the other hand, output to the ADDRESS device sets RAPID to the CREAD mode. Just before completing the RAPID write cycle, which means during the execution, RAPID can be either in the CREAD or the CWRITE mode. The output to the ADDRESS device is executed according to the mode.

- (1) In the CREAD mode: data is transferred from memory to the DATA buffer.
- (2) In the CWRITE mode: data is transferred from the DATA buffer to memory.

Input from the ADDRESS or DATA device will not affect the CREAD mode flipflop.

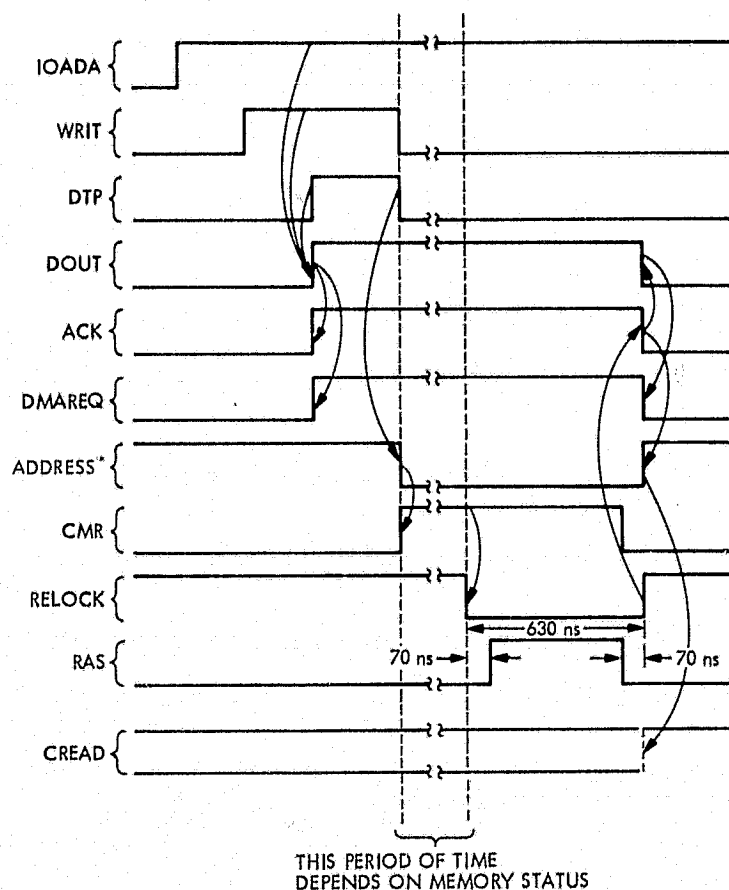


Fig. 11. ADDRESS device output timing

On completion of either the "READ" or "WRITE" cycle, RAPID will be in the CREAD mode. This permits a sequential I/O instruction to the digitizer without having to modify the CREAD flipflop with a control instruction. When the program doesn't complete the RAPID I/O cycle, it must set the CREAD flipflop with the corresponding control instruction.

X. TEST AND CONTROL INSTRUCTIONS TO DIGITIZER

A. TEST INSTRUCTIONS

To ADDRESS device: 000 test is true when interrupt is enabled.

To ADDRESS device: 001 test is true when power is on.

To ADDRESS device: 010 test is true when in half-word mode.

To ADDRESS device: 011 test is true when in CREAD mode.

To ADDRESS device: 100 test is true when picture is completed.

To DATA device: 000 test is true when in no-camera mode.

To DATA device: iii test is true when camera iii is on.

B. CONTROL INSTRUCTIONS

To ADDRESS device: 000 sets interrupt on.

To ADDRESS device: 001 sets interrupt off.

To ADDRESS device: 010 sets half-word mode.

To ADDRESS device: 011 sets full-word mode.

To ADDRESS device: 100 sets CREAD mode.

To DATA device: 000 stops cameras.

To DATA device: iii selects camera iii

C. RAPID INITIALIZATION INSTRUCTION

ADDRD EQU X' ADDRESS device number.

DATAD EQU X' DATA device number.

INTON EQU 0 interrupt on (control instrument number) to ADD device.

INTOF EQU 1 interrupt off (control instrument number) to ADD device.

| | | | |
|------|-----|---|--|
| HWM | EQU | 2 | half word (control instrument number) to ADD device. |
| FWM | EQU | 3 | full word (control instrument number) to ADD device. |
| RM | EQU | 4 | read mode (control instrument number) to ADD device. |
| MSK | EQU | 0 | interrupt in test to ADDRESS device. |
| POW | EQU | 1 | power test to ADDRESS device. |
| HWMT | EQU | 2 | half-word mode test to ADDRESS device. |
| RMT | EQU | 3 | read mode test to ADDRESS device. |

D. I/O TO RAPID

LDV A, 200

LDV B, X'517' Those four instructions are for output to RAPID. In this sample 200 is written to 16-bit address 517, which corresponds to element 5 in horizontal line 23.

DTOR A, DATAD

DTOR B, ADDR D

LDR A, X'517' Those three instructions are for input from RAPID. In this case, content of address 517 is read to Reg B.

DTOR A, ADDR D

DTIR B, DATAD

XI. BLOCK AND LOGIC DIAGRAMS

A block diagram of the RAPID system (Fig. 12) and logic diagrams of the different boards (Figs. 13-18) are presented in this section. The block diagram contains the allocation of the different logic units to the boards. It is hoped that this will make comprehension of the logic diagrams of the boards less difficult.

The diagram illustrates the architecture of the SPC-16 RAID Interface Board, organized into several functional sections:

- Input Section:** Features a 16-bit data bus (D0-D15) connected to a multiplexer (MUX) and a summing junction (Σ). The summing junction also receives input from an ANALOG ENCL. block.
- Processing Section:** Includes an ADC (Analog-to-Digital Converter), a DAC (Digital-to-Analog Converter), and a VIDEO block. The VIDEO block is connected to a VIDEO GEN (Video Generator) and a VIDEO ENCL (Video Encoder/Decoder).
- Timing and Control Section:** Contains a VIDEO TIMING block, a VIDEO CYCLE GENERATOR, and a DATA ENCL (Data Encoder/Decoder).
- Memory Section:** Includes a MEMORY block and a MEMORY ENCL (Memory Encoder/Decoder).
- Data Interface Section:** Features a DATA INTERFACE BUS and a DATA ENCL.
- Addressing Section:** Includes an ADDRESS BUFFER and a VIDEO SELECT AND DATA ADDRESS block.

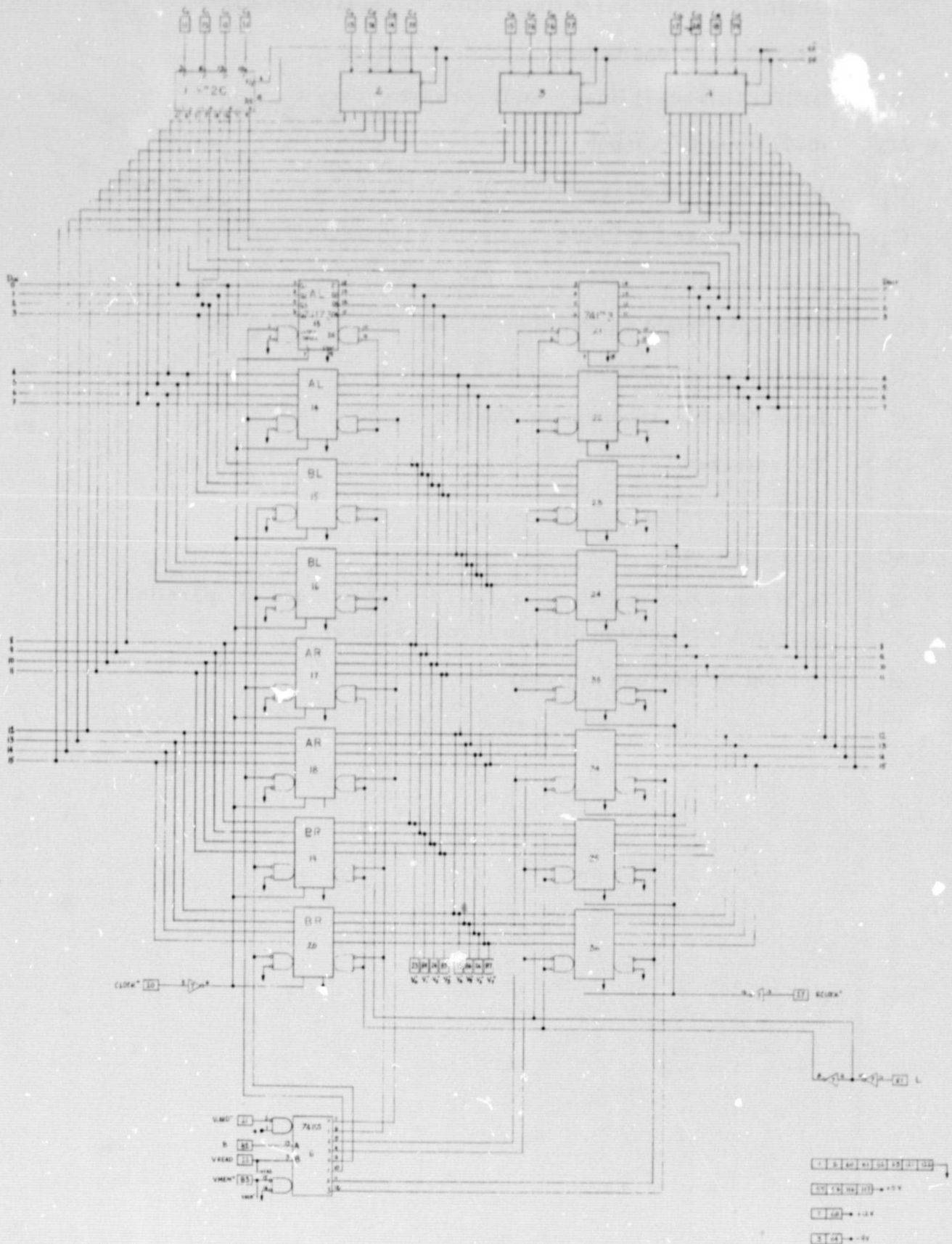
The diagram shows a complex network of data and control lines connecting these blocks, with specific signal paths labeled for timing and data flow.

Fig. 12. RAPID block diagram

RAPID Block Diagram Key

- A OTB(0-15) outbus
- B INB(0-15) inbus
- C FAP, WRIT, DTP, SYRT, READ, IHLD, POLL, IACK, IPSI (standard SPC-16 output control signals)
- D DREQ, IPSO, IPSI, IREQ (standard SPC-16 input control signals)
- E POW, VDRIVE (power-on signal, vertical drive signal)
- F CAM S (0-2) (camera selection)
- G CWRITE, HWORD (computer writing signal, half-word signal)
- H ACK (RAPID is ready for I/O signal)
- I DOUT, DATA, ADDRESS (data out signal, bus control signals)
- J I(0-15) (two-directional data bus)
- K 14-MHz clock
- L CAL, VMEM, RAS, RCLOCK (information for data buffer timing control)
- M ADDRESS (specified whether the next memory cycle is data buffer memory transfer or memory video transfer)
- N CCARD(0-3), ALRAS, ARRAS, BLRAS, BRRAS (chip selection information for computer/memory transfer)
- O C(0-15) (content data bus computer to memory, memory to computer)
- P A(0-5) (6 bits of chip column address or chip raw address)
- Q CAS (column address strobe)
- R L, B, VMEM, VREAD (select card(0, 1, 2, 3) buffer block (A/B) buffer part (L/R) and mode (video input/nonvideo))
- S V(0-1) (digitized pixel to memory or from memory)
- T ARAS, BRAS, VCARD (chip control data for video I/O)
- U A(0-5) (column or raw address of data coming from video)
- V CAMS - CAMERA SELECT (3 lines)

W CBURST - color burst flag (follow the horizontal drive)
 X CSYNC - composite sync
 ZI DIGITIZED (0-7) lines - A/D convertor output
 ZO (0-7) lines D/A input
 C₁ 15-bit data for address data to address device (full word mode)
 C₂ bus to access 8 bit data (left part) to or from RAPID
 C₃ 8-bit data (right part) to or from RAPID
 C₄ 8-bit data (right part to RAPID, left part from RAPID)
 C₅ input data bus transceiver (left 8 bit)
 C₆ input data bus transceiver (right 8 bit)
 DC DC restore
 ADC A/D converter
 DAC D/A converter
 S₁ A/D converter output control according to mode of operation
 (current digitization display from memory)
 S₂ content or address selector



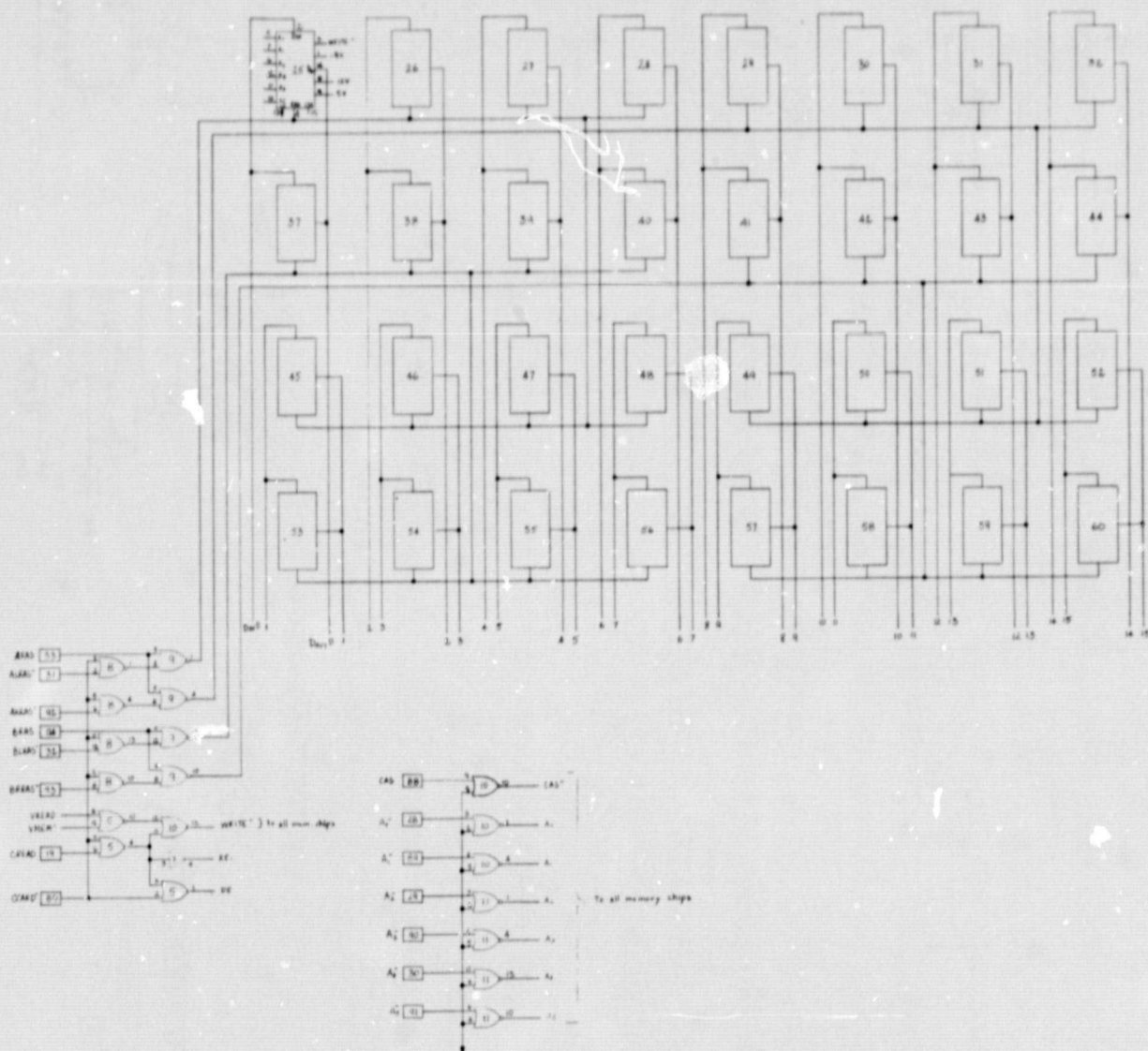
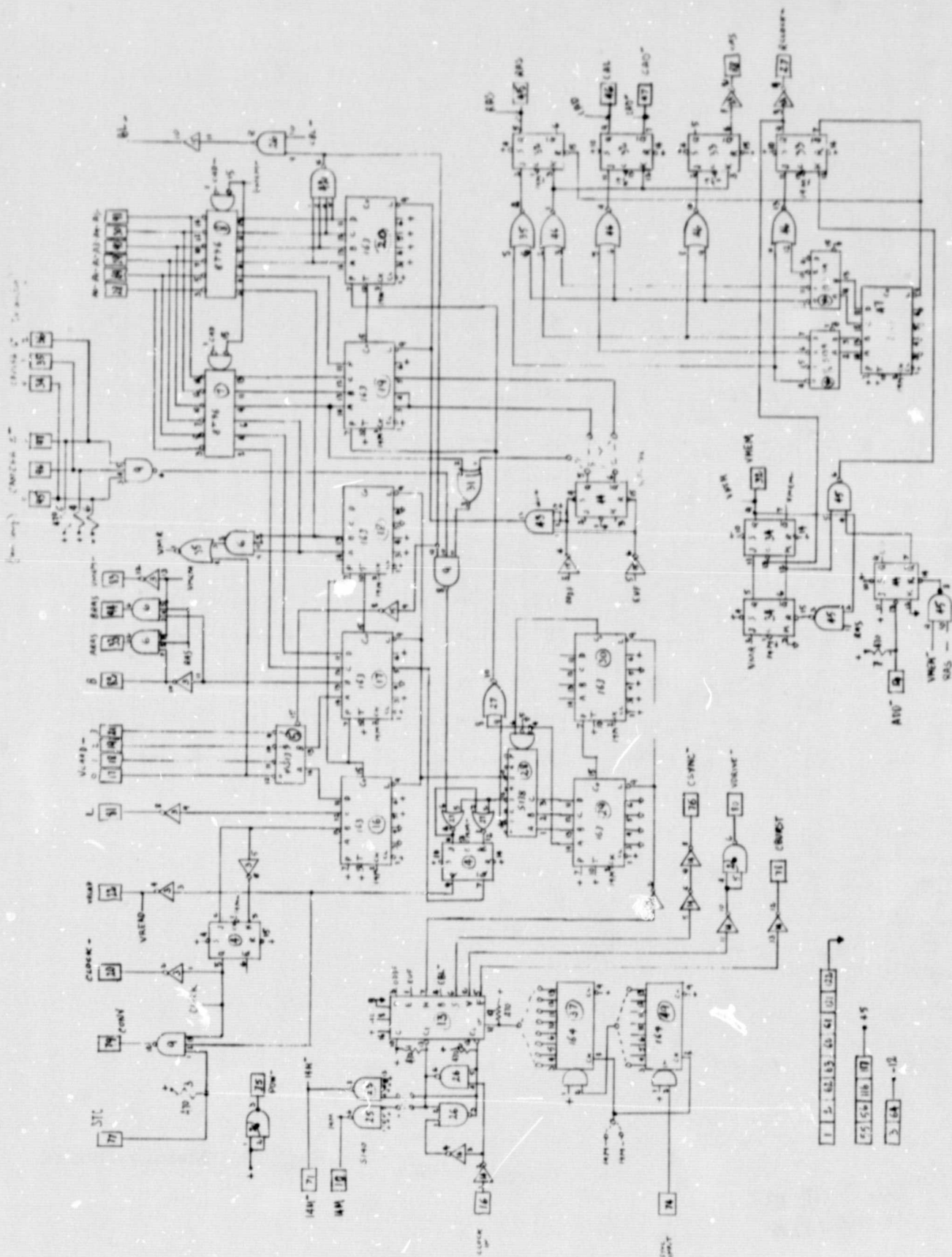


Fig. 13. Memory board

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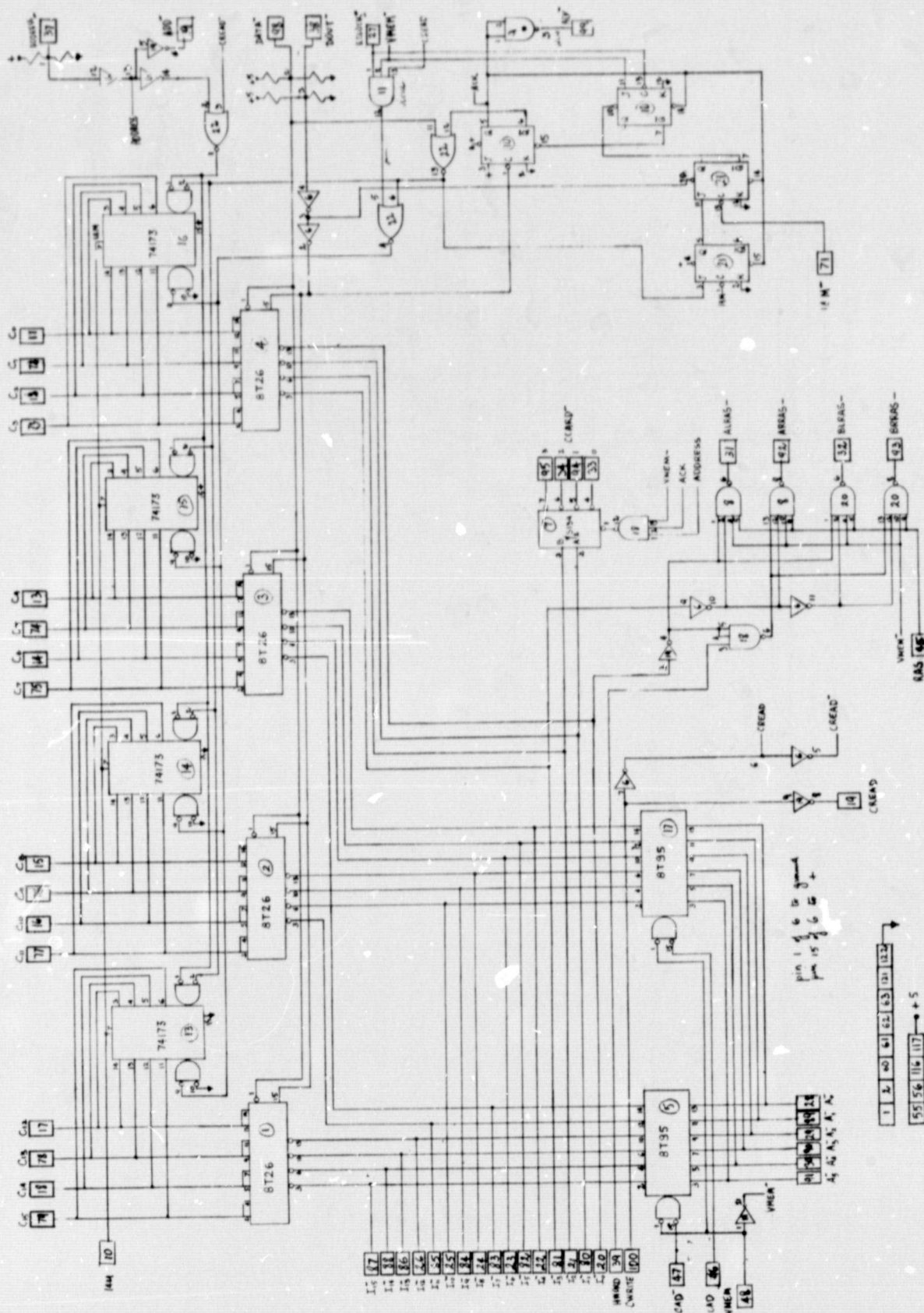


Fig. 16. Data board

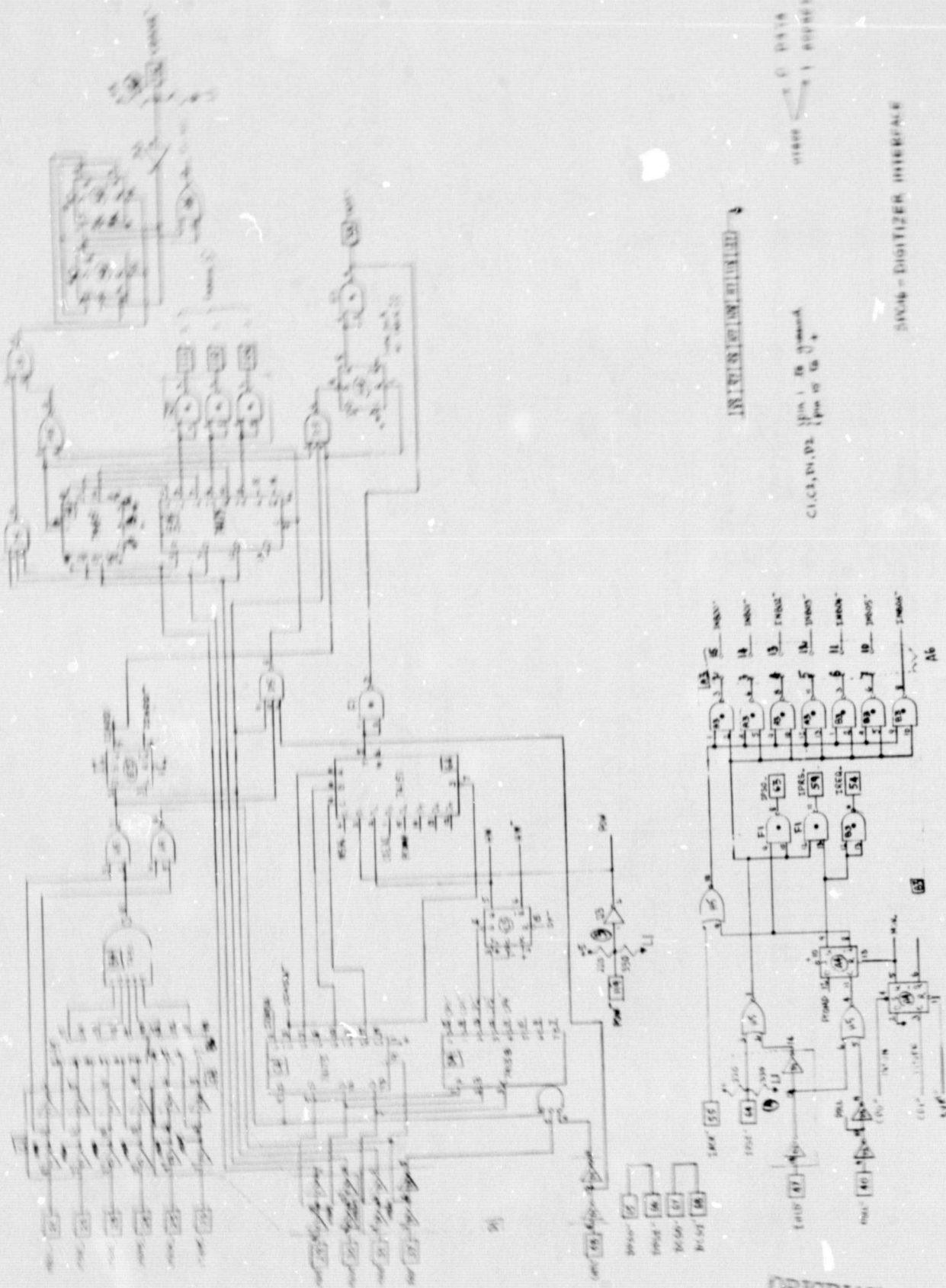


Fig. 17. SPC-16 digitizer interface

